Electronic Version
Stylesheet Version v1.1.1

PIPELINE-BASED CIRCUIT WITH A POST-PONED CLOCK-GATING MECHANISM FOR REDUCING POWER CONSUMPTION AND RELATED DRIVING METHOD THEREOF

Abstract

A pipeline-based circuit with a postponed clock-gating mechanism and related driving method are disclosed for reducing power consumption, and the driving method does not deteriorate processing performance of the pipeline-based circuit. A pipeline-based circuit has a plurality of logic operators cascaded to form at least a pipeline, a pipeline control unit for generating at least a control signal to each logic operator for controlling whether one logic operator needs to pipe data to next logic operator, and a control value calculator for setting a valid bit of each logic operator following a currently activated logic operator according to the control signals generated from the pipeline control unit. When each logic operator begins operating, the related control value is used to determine whether or not a clock signal piping data of the

present logic operator to next logic operator is gated to reduce power consumption. This postponed clock-gating mechanism avoids the degradation of pipeline clock speed limitation.